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FORM PTO-1390 (REV. 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 10191/1614

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
09/720720

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE (26.04.00)	PRIORITY DATE(S) CLAIMED (29.04.99)
PCT/DE00/01295	26 April 2000	29 April 1999

TITLE OF INVENTION
METHOD FOR ELIMINATING DEFECTS IN SILICON ELEMENTS THROUGH SELECTIVE ETCHING

APPLICANT(S) FOR DO/EO/US

SPITZ, Richard; UEBBING, Helga; EIMERS-KLOSE, Doerte; LAERMER, Franz; SCHILP, Andrea

Applicant(s) herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) immediately rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (unsigned).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: International Search Report and Form PCT/RO/101.

Express Mail No. EL302702565

U.S. APPLICATION NO. If known, see 37 C.F.R.1.5	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/720720	PCT/DE00/01295	10191/1614

17. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	15 - 20 =	0	X $18.00	$ 0	
Independent Claims	1 - 3 =	0	X $80.00	$ 0	
Multiple dependent claim(s) (if applicable)			+ $270.00	$ 0	
			TOTAL OF ABOVE CALCULATIONS =	$ 860	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
			SUBTOTAL =	$ 860	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).			+	$	
			TOTAL NATIONAL FEE =	$ 860	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property			+	$	
			TOTAL FEES ENCLOSED =	$ 860	
			Amount to be: refunded	$	
			charged	$	

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of $860.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kenyon & Kenyon
One Broadway
New York, New York 10004

By Reg No 35,952
SIGNATURE

Richard L. Mayer, Reg. No. 22,490
NAME

12/28/00
DATE

330377

[10191/1614]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Richard SPITZ et al.
Serial No.	:	To Be Assigned
Filed	:	Herewith
For	:	METHOD FOR ELIMINATING DEFECTS IN SILICON ELEMENTS THROUGH SELECTIVE ETCHING
Art Unit	:	To Be Assigned
Examiner	:	To Be Assigned

Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

SIR:

Please amend the above-identified application before examination, as set forth below.

IN THE SPECIFICATION:

Page 1, before line 1, insert:

--FIELD OF THE INVENTION--.

Page 1, line 4, change "wafer according to the" to --wafer.--.

Page 1, delete line 5.

Page 1, delete line 7.

Page 1, before line 9, insert:

--BACKGROUND INFORMATION--.

Page 1, line 9, delete "known".

Page 1, line 9, change "is to cut" to --involves cutting--.

Page 1, line 17, change "a manner that is known per se" to --an available manner--.

Page 1, line 22, change "often results" to --may result--.

Page 1, line 29, delete "known".

Page 2, line 1, change "The" to --In such methods, the--.

Page 2, lines 1 and 2, change "is then" to --may be--.

Page 2, line 6, delete "The latter object is".

Page 2, delete line 7.

Page 2, line 9, change "there" to --it is believed that there--.

Page 2, line 10, change "The" to --The available--.

Page 2, line 11, delete "frequently used today".

Page 2, line 19, change "currently known" to --available--.

Page 2, line 22, change "methods" to --available methods--.

Page 2, lines 22 and 23, delete "known from the related art".

Page 2, line 24, change "are described" to --include--.

Page 2, line 32, change "the known method" to --these methods--.

Page 3, delete line 4.

Page 3, before line 6, insert:
--SUMMARY OF THE INVENTION--.

Page 3, delete lines 6 to 8, and insert:
--The exemplary method according to the present invention is believed to have the advantage that it can be used to etch silicon--.

Page 3, line 16, change "method" to --exemplary method--.

Page 3, line 16, change "further" to --believed to be further--.

Page 3, line 20, delete "known".

Page 3, line 23, change "method" to --exemplary method--.

Page 3, line 30, change "method" to --exemplary method--.

Page 3, line 36, change "method" to --exemplary method--.

Page 4, line 3, change "method" to --exemplary method--.

Page 4, line 10, delete "great".

Page 4, line 10, change "is" to --is believed to be--.

Page 4, line 12, change "method" to --exemplary method--.

Page 4, delete lines 22 and 23.

Page 4, line 25, change "method" to --exemplary method--.

Page 4, line 35, change "method" to --exemplary method--.

Page 5, line 18, change "method" to --exemplary method--.

Page 5, line 23, change "method" to --exemplary method--.

Page 5, line 29, change "advantageously suitable" to --exemplary--.

Page 5, line 30, change "is to wash" to --includes washing--.

Page 6, delete line 5.

Page 6, before line 7, insert:
--DETAILED DESCRIPTION--.

Page 6, line 7, change "method" to --exemplary method--.

Page 6, line 16, change "of a" to --of any--.

Page 6, line 17, change "reactor" to --suitably appropriate reactor--.

Page 6, line 17, change "that is known per se".

Page 6, lines 25 and 26, delete ", which is known per se,".

Page 7, line 8, change "known per se" to --available--.

Page 7, line 9, change "commonly" to --may be--.

Page 7, lines 21 and 22, delete "it is preferable to use".

Page 7, line 22, change ", in which" to --may be used, in which--.

Page 8, line 4, change "method" to --exemplary method--.

Page 8, line 9, change "a manner that" to --an available manner--.

Page 8, line 10, delete "is known per se,".

Page 8, line 13, change "with an" to --using an available--.

Page 8, line 13, change "plating" to --plating method.--.

Page 8, delete line 14.

Page 8, delete line 17, and insert --available flexible sawing sheet, made--.

Page 8, line 19, delete "a".

Page 8, delete line 20, and insert --an available sawing method into silicon--.

Page 8, line 26, change "according to" to --according to an exemplary method of--.

Page 8, line 32, change "is preferably" to --may be--.

Page 8, line 35, change "is preferably" to --may be--.

Page 9, line 3, change "is preferably" to --may be--.

Page 10, delete line 12, and insert --particular spin-coating, an available lacquer layer--.

Page 11, line 21, change "known per" to --available.--.

Page 11, delete line 22.

Page 11, line 27, change "preferably" to --which may be--.

Page 12, line 3, change "preferably" to --which may be--.

Page 12, line 32, change "a manner that is' to --an available manner.--.

Page 12, line 33, delete "known per se.".

Page 12, line 33, delete "a".

Page 12, delete line 34, and insert --an available manner to ensure the stability of--.

IN THE ABSTRACT:

Delete lines 1 to 14, and insert:

-- ABSTRACT OF THE DISCLOSURE

A method for eliminating eruptions, impurities, and/or damage in a crystal lattice by selectively etching silicon elements of surface-plated and sawn-out parts of a silicon wafer. At least areas of the silicon elements are brought into contact with a gaseous etching medium that etches silicon selectively in a chemical reaction, and gaseous reaction products are produced during etching. An interhalogen or fluorine-noble gas compound that is in a gaseous state or was converted to the gaseous phase may be used as the etching medium. The method is believed to be suitable for producing power diodes sawn from a wafer or for overetching fully mounted individual diodes.--.

IN THE CLAIMS:

On the first page of the claims, first line, change "Patent Claims" to:
--WHAT IS CLAIMED IS:--.

Please cancel original claims 1 to 15, without prejudice, and please add new claims 16 to 30 as follows:

--16. (New) A method for substantially eliminating at least one of eruptions, impurities and damage in a crystal lattice, the method comprising the steps of:

providing a surface-plated, sawn-out part of a silicon wafer; and

selectively etching at least one silicon element of the surface-plated, sawn-out part of the silicon wafer by bringing at least an area of the at least one silicon

element into contact with a gaseous etching medium for etching silicon selectively in a chemical reaction, wherein gaseous reaction products are produced during the step of selectively etching.

17. (New) The method of claim 16, wherein the gaseous etching medium includes one of an interhalogen compound, which is one of in a gaseous state and has been converted to the gaseous state, and a fluorine-noble gas compound, the fluorine-noble gas compound including at least one of chlorine trifluoride, bromine trifluoride, iodine pentafluoride and xenon difluoride.

18. (New) The method of claim 16, wherein the gaseous reaction products include silicon tetrafluoride.

19. (New) The method of claim 16, wherein the step of selectively etching is performed at a pressure of 0.1 mbar to 1,000 mbar.

20. (New) The method of claim 16, wherein the gaseous etching medium is diluted with at least one of an inert gas and helium to control at least one of an aggressiveness of the gaseous etching medium and an etching rate.

21. (New) The method of claim 16, wherein at least a part of the gaseous etching medium is one of: convertable from a solid phase to the gaseous phase by thermal sublimation using a solid source; convertable from a liquid phase to the gaseous phase by introducing an inert gas using a bubbler; and convertable from one of the liquid phase and the solid phase to the gaseous phase based on a vapor pressure at a defined temperature.

22. (New) The method of claim 16, wherein the at least one silicon element is sawn from the silicon wafer prior to performing the step of selectively etching.

23. (New) The method of claim 22, wherein the silicon wafer is attached to a carrier, and the carrier is a sawing sheet clamped into a frame.

24. (New) The method of claim 22, wherein the at least one silicon element is initially left on a carrier after the at least one silicon element has been sawn out and treated while still attached to the carrier.

25. (New) The method of claim 24, further comprising the step of expanding the sawing sheet after sawing out the plurality of silicon elements and before performing the step of selectively etching to increase a distance between the at least one silicon element and another silicon element, wherein the frame is used as an expansion frame for the sawing sheet.

26. (New) The method of claim 23, further comprising the step of drying the at least one silicon element before performing the step of selectively etching by heating the at least one silicon element with a radiation heater in a vacuum at a pressure of less than about 0.1 μbar.

27. (New) The method of claim 16, further comprising the step of adjusting an etching rate while selectively etching the at least one silicon element by selecting at least one of the gaseous etching medium, a composition of the gaseous etching medium and an etching temperature.

28. (New) The method of claim 16, further comprising the step of removing the gaseous reaction products produced during the step of selectively etching at least one of during the step of selectively etching and after the step of selectively etching.

29. (New) The method of claim 16, further comprising the step of removing, after performing the step of selectively etching in a reaction chamber, at least one of a leftover etching medium and a leftover reaction product from at least one etched silicon element in a vacuum in a load lock, the step of removing being performed at a pressure of less than about 0.1 μbar and at an elevated temperature.

30. (New) The method of claim 16, wherein the step of selectively etching includes selectively etching an edge of a power diode.--.

Remarks

This Preliminary Amendment cancels, without prejudice, original claims 1 to 15 in the underlying PCT Application No. PCT/DE00/01295, and adds new claims 16 to 30. The new claims conform the claims to U.S. Patent and Trademark Office rules and do not add new matter to the application.

The above amendments to the specification and abstract are to conform the specification and abstract to U.S. Patent and Trademark Office rules or to correct informalities, and do not introduce new matter into the application.

The underlying PCT Application No. PCT/DE00/01295 includes an International Search Report, dated September 22, 2000. The Search Report includes a list of documents that were uncovered in the underlying PCT Application. A copy of the Search Report accompanies this Preliminary Amendment.

Applicants assert that the subject matter of the present application is new, non-obvious, and useful. Prompt consideration and allowance of the application are respectfully requested.

Respectfully Submitted,
KENYON & KENYON

Dated: 12/28/00

By: [signature] Reg. No. 35,952
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330192

METHOD FOR ELIMINATING DEFECTS IN SILICON ELEMENTS THROUGH SELECTIVE ETCHING

The present invention relates to a method for eliminating eruptions, impurities, and/or damage in the crystal lattice by selectively etching silicon elements, in particular of surface-plated parts of a silicon wafer, according to the definition of species in Claim 1.

Background Information

A known method for producing silicon power diodes is to cut a number of individual diodes from a silicon wafer that has been doped on both sides with an n- or p-type dopant in full-surface doping steps to generate a pn junction and subsequently plated all over on both sides, by first sawing the entire wafer into squares or hexagons measuring roughly 5 x 5 mm^2 and then suitably building up and electrically bonding such individual silicon surface diodes. The silicon wafer is doped and plated in a manner that is known per se, with the surface plating layer being made, for example, of a chromium-nickel-vanadium-silver alloy (CrNiVAg).

The sawing step, which is necessary to produce individual diodes from the silicon wafer, often results in irregular eruptions on the sawn edge or impurities and damage in the crystal lattice so that the pn junctions in the sawn-out individual diodes are partially or regionally damaged. This damage then leads to higher leakage currents, which, in the end, renders the created diode unusable at this stage.

Therefore, in known methods for producing silicon power diodes of this type, the sawing step must be followed by a wet-chemical overetching of the diodes, thus stripping the damaged silicon areas and restoring a suitably intact crystal lattice in the pn junction region.

The chemical etch-stripping of the damaged silicon areas is then followed by passivation of the exposed silicon edge to protect the pn junctions against environmental influences and to reliably prevent the electronic properties from again deteriorating over the life of the diode. The latter object is considered to be achieved by the related art.

However, there are at present no satisfactory means of etch-stripping the damaged silicon areas at the sawn edge. The wet-chemical etching method frequently used today results, for example, in unfavorable etching profiles with greater risk of electrical breakdown, due to its pronounced doping selectivity, as well as in disadvantageous yields, due to occasional rejects during etching. In addition, the etching profile produced by wet-chemical etching also reduces the diode's mechanical stability.

Furthermore, according to the currently known methods, only the fully mounted diodes are exposed to the aqueous etching solution, which involves expensive handling of the individual diodes. To summarize, therefore, the methods known from the related art for overetching silicon elements sawn out of a silicon wafer are described by the following process steps:

Wet-chemical etching of the sawn-out silicon elements, i.e., diodes, mounting of the diodes, immersion of the mounted diodes in etching baskets into etching basins, neutralization of the etching solution, and subsequent thorough rinsing and drying of the diodes.

The agents needed for the known method are an etching solution, a neutralization solution, and hydrogen peroxide, resulting in serious environmental pollution due to the materials used as well as high energy consumption and the use of de-ionized water. Thus, wet-etching takes place, for

example, at temperatures above 90°C, and a rinsing cascade is needed for subsequent cleaning of the etched, mounted diodes.

Advantages of the Invention

The method according to the present invention having the characterizing features of the main claim has the advantage over the related art that it can be used to etch silicon elements, in particular surface-plated, sawn-out parts of a silicon wafer, using a gaseous etching medium that selectively etches almost exclusively silicon through a chemical reaction, thus producing gaseous reaction products. During this selective etching process, surface eruptions and/or impurities, and/or damage in the crystal lattice of the silicon element, in particular, are eliminated at the same time. The method according to the present invention is further advantageously suitable for stripping damaged silicon zones, in particular of sawn-out silicon elements, like those that occur, for example, when producing silicon power diodes. It is reliable, economical, and overcomes the known disadvantages of fluid etching media.

One particular advantage is that the method according to the present invention is a "batch process", i.e., a process on the wafer level. Thus, one particular advantage is that the individual chips do not need to be handled, which means that all sawn-out silicon elements, i.e., chips, of a wafer can be etched simultaneously, which saves a great deal of space and requires only one process step, i.e., handling step. If necessary, the method according to the present invention can also be used to overetch fully mounted individual diodes, as is currently the case. In doing this, it is necessary only to replace the wet-etching process that is known per se with an etching process using a gaseous etching medium.

A further advantage is that the method according to the present invention for selective etching does not use a fluid,

thus achieving a clean gas-phase etching of the silicon elements that have been, in particular, sawn out. Moreover, the method according to the present invention is also less selective toward doping concentrations, resulting in advantageous etched edge profiles and, in particular, prevents a "boron balcony" from forming on the sawn-out and overetched diodes, at the same time increasing mechanical stability and reducing failure rates.

Another great advantage is the selective removal of damaged silicon zones, eruptions or impurities, as well as the planarizing effect of the method according to the present invention. Due to the high selectivity of the gaseous etching medium used and the chemical reaction that this produces on the surface of the silicon element, and particularly due to the selectivity of this reaction on damage in these zones, it is possible to etch-strip significantly more material, with damaged areas automatically undergoing more aggressive etching, particularly in the edge areas of the sawn-out silicon elements.

Advantageous embodiments of the present invention are provided by the features mentioned in the subclaims.

Thus, the method according to the present invention offers the advantage that the etching rates can be selectively adjusted, for example via the composition of the gaseous etching medium. This makes it possible to set, if necessary, low etch-stripping rates, thereby increasing reproducibility and thus reducing overall process time. However, it is also possible to set very high etching rates, particularly when using chlorine trifluoride or bromine trifluoride, and thus significantly shorten the actual etching time.

The very high selectivity of the method according to the present invention toward non-silicon materials is due to a surface-catalytic initiation of the etching reaction, so that

a large number of materials are also advantageously suitable for use as the etching mask.

For example, even a surface-plating of the silicon wafer, which serves as the later diode plating, can be used as the etching mask while etching with the gaseous etching medium without this plating itself being significantly corroded. Another advantage in this regard is that a sawing sheet used and an adhesion layer provided between this sawing sheet and the silicon wafer attached to it are also not significantly corroded, due to the high selectivity of the etching medium toward non-silicon materials. Furthermore, an additional lacquer layer can be advantageously applied all over in a manner that is known per se, for example by spin-coating, thus further protecting the surface plating of the silicon wafer.

In the case of the interhalogen or fluorine-noble gas compounds suitable for the method according to the present invention, suitable process conditions further ensure that no free chlorine, bromine or iodine occurs, leaving only a very low risk of corrosion after completion of the etching process.

Further advantages of the method according to the present invention include low energy consumption because there is no need to heat, for example, the diodes or etching baths, low chemical consumption, and environmental compatibility. For example, any waste gases produced can be very easily disposed of without harmful effects through after-treatment, eliminating hazardous waste. An advantageously suitable method is to wash the waste gases in lime water, i.e., an aqueous calcium hydroxide solution in a "gas washer" ($Ca(OH)_2 + 2HF \rightarrow CaF_2\downarrow + 2\ H_2O$).

Chlorine trifluoride, bromine trifluoride, iodine pentafluoride, or xenon difluoride that are in a gaseous state or have been converted to the gaseous phase, or a mixture of

these compounds, are particularly suitable as the etching medium. In this case, silicon tetrafluoride, for example, is produced as the reaction product.

Description of Embodiments

The method according to the present invention for eliminating eruptions, impurities, or damage in the crystal lattice of silicon elements by selective etching of silicon generally makes use of the characteristic of certain fluorine compounds, known as interhalogens or fluorine-noble gas compounds, to spontaneously etch silicon, i.e., through contact between the fluorine compound and silicon, where this etching action takes place from the gaseous phase, and gaseous reaction products are produced. To do this, a gaseous silicon-etching fluorine compound, for example, is supplied to a reaction chamber of a reactor that is known per se, in which the silicon elements to be etched were previously placed. Adsorption of the gas molecules of the gaseous etching medium on the accessible silicon surfaces results in spontaneous, surface-catalytic fragmentation of the etching medium used, thus releasing fluorine radicals that react with the silicon to form a volatile product, for example SiF_x (x = 2, 3, 4). The best known product of a reaction of this type is, for example, stable silicon tetrafluoride SiF_4. The mechanism, which is known per se, can be described as follows, where X is Cl, Br, I or Xe, and n is the number of fluorine atoms in the particular compound:

1. Adsorption: $XF_n \rightarrow XF_n^{adsorb}$

2. Surface-catalytic decomposition: $XF_n^{adsorb} \rightarrow XF_{n-1}^{adsorb} + F^{*,adsorb}$

3. Chemical transformation: $Si + xF^{*,adsorb} \rightarrow SiF_x$ (x = 1, 2, 3, 4)

4. Desorption of reaction products: $SiF_x \rightarrow SiF_x\uparrow$ (x = 2, 3, 4)

in particular: $Si + 4F^{*adsorb} \rightarrow siF_4\uparrow$

Examples of suitable compounds of the XF_n type are the interhalogen compounds chlorine trifluoride, bromine trifluoride and iodine pentafluoride, as well as the noble gas fluoride xenon difluoride. The chlorine trifluoride and bromine trifluoride compounds are known per se in the semiconductor industry, where they are commonly used to clean wafers or wafer handling devices.

While chlorine trifluoride and bromine trifluoride are liquids with a vapor pressure of 1 bar at 150°C, iodine pentafluoride is a semiliquid, and xenon difluoride is a solid with a vapor pressure of approximately 20 mbar and 2 mbar, respectively, at 15°C. Thus chorine trifluoride and bromine trifluoride can be taken directly from a gas bottle, due to their high vapor pressure, while iodine pentafluoride and xenon difluoride must first be converted to the gaseous phase, using a suitable vaporizing apparatus, preferably at an elevated temperature. When using the liquid iodine pentafluoride, it is preferable to use a "bubbler", in which the liquid is "bubbled" with an inert gas, for example helium, as the carrier gas, and the gas mixture is then supplied to the reaction chamber.

In the case of the interhalogen compounds chlorine trifluoride and bromine trifluoride, stripping takes place in a first reaction step of the etching reaction, in which fluorine radicals are released to form stabile chorine fluoride (ClF) and unstable bromine fluoride (BrF), respectively, with two fluorine radicals being generated in each case.

In the case of iodine pentafluoride, the medium is first converted to the relatively stable iodine trifluoride, and in the case of the noble gas fluoride xenon difluoride,

elementary xenon is formed in addition to the two fluorine radicals.

When carrying out the method according to the present invention, one embodiment begins with a silicon wafer from which silicon power diodes are to be produced, with one side of the wafer being doped with an n-type dopant in a manner that is known per se, using an all-over doping step, and the other side being doped with a p-type dopant in a manner that is known per se, using an all-over doping step. A pn-junction thus forms over the entire interior of the silicon wafer. Afterwards, the wafer that has been pretreated in this manner is provided on both sides with an all-over CrNiVAg plating that is known per se.

This silicon wafer is then attached to a commercially available, flexible sawing sheet, which is known per se, made for example from polyvinyl chloride (PVC) or polycarbonate, using an adhesion layer provided on it, and sawn using a sawing method in a manner that is known per se into silicon elements measuring approximately 5 x 5 mm^2 and shaped like squares or hexagons, with the silicon elements being used as silicon power diodes at the end of the manufacturing process.

After the wafer has been sawn, the sawn-out silicon elements produced are first treated, according to the present invention, while still attached to the sawing sheet, which means that no individual chips are yet produced at this stage, but only an entire unit of sawn-out silicon elements.

To ensure mechanical stability, the edge of the sawing sheet is preferably clamped in a fixed frame during sawing and during the course of the remaining process steps, so that it can be gripped with particular ease and treated automatically. After the wafer has been sawn, the sawing sheet is preferably first expanded to increase the distance between the silicon elements and thus give the gaseous etching medium used later

on, for example chorine trifluoride, better access to the side walls of the individual sawn-out silicon elements. An expansion frame is preferably used for this purpose, forming a stable frame for handling the otherwise flexible sawing sheet.

In any case, it is important to carefully dry the sawn-out silicon elements after sawing the silicon wafer and expanding the sawing sheet, but before etching. This ensures that no moisture enters the reaction chamber of the reactor used later to carry out the actual selective etching of the silicon elements.

In doing this, it is advisable to load the sawn-out silicon elements that have been placed on the sawing sheet and are joined to the wafer into the reaction chamber of the reactor using a loading device, such as a load lock, which includes an evacuation and heating function, for example a radiation heater using corresponding lamps.

Pumping out the loading device to create a vacuum and simultaneously heating the wafer that was sawn into silicon elements and is located on the sawing sheet in the loading device, for example using a radiation heater, removes remnants of moisture particularly efficiently before the wafer that was sawn into silicon elements enters the actual reaction chamber of the reactor, where the described etching reaction takes place after introducing the gaseous etching medium. The presence of moisture greatly encourages corrosion effects at this stage and is therefore undesirable.

To release fluorine radicals, the etching gases used require surface-catalytic decomposition that takes place only in connection with the actual etching reaction with the silicon, which means that the etching reaction is extraordinarily highly selective with respect to non-silicon materials. As a result, the etching conditions can be very easily set, for example by selecting a gaseous etching medium and

concentration so that only the silicon surfaces, but not metals or plastics, are significantly corroded by the etching chemicals used.

Thus metal layers, in particular applied surface plating, as well as the sawing sheet used fully satisfy the requirements that an etching reaction mask must meet to strip only a sawn edge damaged during sawing, but not the entire silicon surface. If additional protection of the surface plating or metal layers against even minor etching corrosion is required, this can be easily accomplished by additionally applying, in particular spin-coating, a lacquer layer that is known per se onto preferably the entire surface of the silicon wafer.

After the sawn silicon wafer, which has been attached to the sawing sheet and dried, enters the reaction chamber of the reactor, the gaseous etching medium is then introduced into this chamber. When using the interhalogen compounds chlorine trifluoride or bromine trifluoride, the medium is introduced through flow regulators or throttle valves that are known per se, where the process pressure can range from a low-pressure range, i.e., vacuum, to an atmospheric pressure range. Both of the gases mentioned can be used, for example, in conjunction with a process in the pressure range from 0.1 to 1,000 mbar under controlled flow conditions.

If the process is to take place at higher pressures, it is advantageous to dilute the reactive gas with an inert gas, for example helium. Diluting the gas with helium by a factor of 10 to 100 further makes it possible to very easily control the etching reaction and the etching rate and reduce the aggressiveness of the gaseous etching medium used, which also reduces the potential chemical corrosion of gas lines and the interior of the reaction chamber.

By using a diluted inert gas, it is further possible to work even at atmospheric pressure by limiting the partial pressure,

for example of chlorine trifluoride or bromine trifluoride, to a range of some 10 mbar by correspondingly diluting these gases with helium, which is still sufficient for maximum etching rates, yet also allows the etching process to be efficiently controlled through the inflow of the etching species.

When using the noble gas fluoride xenon difluoride, the latter must first be thermally sublimed from a solid source. In this case, the process pressure when etching the sawn-out silicon elements is thus limited to the vapor pressure of xenon difluoride at the selected working temperature, for example 2 mbar at 20°C.

If iodine pentafluoride is used as the etching medium, the latter must first be converted to the gaseous phase in an evaporator, which limits the working pressure to approximately 20 mbar. Alternatively, however, one can also use a "bubbler" to "bubble" the liquid iodine pentafluoride with an inert gas, for example helium, and supply the gas mixture diluted in this manner to the reaction chamber. Both procedures are known per se to those skilled in the art.

After introducing the gaseous etching medium into the reaction chamber, the actual etching of the sawn-out silicon elements begins, where specifically the damaged areas in the crystalline structure, known as damage zones, preferably on the sawn edge are stripped, and the sawn surfaces are planarized.

The gaseous reaction products produced from the reaction between the gaseous etching medium used and the silicon surfaces are either pumped away continuously, if a throughflow system is used, or accumulate in a reaction chamber that is filled once and then closed, until all gaseous substances are finally pumped out of the reaction chamber upon completion of silicon element etching.

In any case, pumping must continue for a sufficiently long period, and the discharge pressure during pumping must be low enough, preferably less than 0.1 μbar, to ensure that the reaction chamber no longer contains any leftover etching gas before the silicon elements sawn out of the silicon wafer and located on the sawing sheet are discharged from the reaction chamber of the reactor either through the load lock or via the loading device.

When discharging the elements, it is further suitable to also provide a vacuum in the load lock between the reaction chamber and the surrounding atmosphere. This vacuum preferably has a pressure of less than 0.1 μbar, which can be easily achieved by using a turbomolecular pump.

In doing this, the wafer that has been sawn into silicon elements and is attached to the sawing sheet is preferably reheated in the load lock after etching, for example using a radiation heater. This removes as much leftover etching species as possible before the wafer is removed from the load lock, i.e., leftover gaseous etching medium or leftover gaseous reaction products from the sawn-out, overetched silicon elements or from their surfaces affected by etching.

Leftover media of this type remaining on the surface of the silicon element would result in corrosion when exposed to air, due to the effect of moisture in the air.

After the processed silicon elements have been discharged from the reactor, they are finally removed individually from the sawing sheet and built up into diodes in a manner that is known per se. The silicon edges are then passivated in a manner that is also known per se to ensure the stability of the pn junctions and the high performance of the silicon power diodes over their life cycles.

Patent Claims

1. A method for eliminating eruptions, impurities and/or damage in the crystal lattice by selectively etching at least one silicon element, in particular of surface-plated, sawn-out parts of a silicon wafer, characterized in that at least areas of the silicon element are brought into contact with a gaseous etching medium that etches silicon selectively in a chemical reaction, with gaseous reaction products being produced during etching.

2. The method according to Claim 1, characterized in that the etching medium contains an interhalogen compound that is in a gaseous state or was converted to the gaseous phase or a fluorine-noble gas compound, in particular chlorine trifluoride, bromine trifluoride, iodine pentafluoride, xenon difluoride, or a mixture of these compounds.

3. The method according to Claim 1, characterized in that the reaction product is silicon tetrafluoride.

4. The method according to Claim 1, characterized in that etching is carried out at a pressure of 0.1 mbar to 1,000 mbar.

5. The method according to Claim 1, characterized in that the gaseous etching medium is diluted with an inert gas, in particular helium, to control the etching medium aggressiveness and/or the etching rate.

6. The method according to Claim 1, characterized in that the etching medium or part of the etching medium is converted from the solid phase to the gaseous phase by thermal sublimation, using a solid source; or is converted from the liquid phase to the gaseous phase by introducing an inert gas, using a bubbler; or is converted from the liquid or solid phase to the

gaseous phase based on its vapor pressure at a defined temperature.

7. The method according to Claim 1, characterized in that the silicon element or a multiplicity of silicon elements are sawn from a silicon wafer prior to etching.

8. The method according to Claim 7, characterized in that the silicon wafer is first attached to a carrier, in particular a sawing sheet clamped into a frame.

9. The method according to Claim 7 or 8, characterized in that the silicon elements are initially left on the carrier, in particular the sawing sheet, after they have been sawn out and treated while still attached to the carrier.

10. The method according to Claim 9, characterized in that the sawing sheet is expanded after sawing out the silicon elements and before selective etching to increase the distance between the silicon elements, with the frame being used as an expansion frame for the sawing sheet.

11. The method according to Claim 8, characterized in that the sawn-out silicon elements are dried before selective etching, in particular by heating them with a radiation heater in a vacuum at a pressure of less than 0.1 μbar.

12. The method according to at least one of the preceding claims, characterized in that the etching rate while etching the silicon element is adjusted by selecting the etching medium, and/or the etching medium composition, and/or the etching temperature.

13. The method according to at least one of the preceding claims, characterized in that the gaseous reaction products produced during etching are removed during and/or after etching the silicon elements.

14. The method according to at least one of the preceding claims, characterized in that, after etching in a reaction chamber, leftover etching medium or leftover reaction products are removed from the etched silicon elements in a vacuum in a load lock, in particular at a pressure of less than 0.1 μbar and at an elevated temperature.

15. The use of the method according to at least one of the preceding claims to etch the edges of power diodes.

Abstract

A method for eliminating eruptions, impurities, and/or damage in the crystal lattice by selectively etching silicon elements, in particular of surface-plated and sawn-out parts of a silicon wafer. At least areas of the silicon elements are brought into contact with a gaseous etching medium that etches silicon selectively in a chemical reaction. Gaseous reaction products are produced during etching. An interhalogen or fluorine-noble gas compound that is in a gaseous state or was converted to the gaseous phase is particularly suitable as the etching medium. The proposed method is especially suitable for producing power diodes sawn from a wafer or for overetching fully mounted individual diodes.

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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **METHOD FOR ELIMINATING DEFECTS IN SILICON ELEMENTS THROUGH SELECTIVE ETCHING**, the specification of which was filed as PCT International Application No. **PCT/DE00/01295** on April 26, 2000.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

Number	Country filed	Day/month/year	Priority Claimed Under 35 USC 119
199 19 471.8	Fed. Rep. of Germany	29 April 1999	Yes

And I hereby appoint Richard L. Mayer (Reg. No. 22,490) and Gerard A. Messina (Reg. No. 35,952) my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful and false statements may jeopardize the validity of the application or any patent issued thereon.

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